AND8301/D

EMC Specifications and PCB Guidelines for SMPS Devices

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Introduction

Electromagnetic compatibility (EMC) is a very important consideration in modern electronic design. With critical information being transmitted, received, stored and acted upon, accurate communication within and between such devices must be assured. Alongside the continuously increasing power levels and frequencies, engineers must design with EMC in mind, especially in the case of high−density layouts.

Switch−mode power supplies (SMPS) are critical power management components in many automotive applications.

The purpose of this document is to explain the EMC testing procedure with specific regard to SMPS applications. Universal standards as well as company standards are described in detail, along with printed circuit board (PCB) design guidelines for reference.

EMC Background

Electromagnetic compatibility (EMC) is the capability of a particular electronic component to function properly under its normal operating conditions without disturbing, or being disturbed by, the operation of any other components or devices. More specifically, electromagnetic susceptibility (EMS) is the level of tolerance of an electronic component or device to various forms of electromagnetic radiation. Electromagnetic interference (EMI) is the level of electromagnetic radiation that is emitted from the device in operation.

There is a set of accepted standards that regulates the amount of radiation a device must be able to withstand as well as the amount that it is allowed to emit. Under a strict method of EMC testing, the final revision of a component must meet these requirements in order to be suitable for a particular application.

Three standards are commonly used for EMC applications: IEC62132−4 (*Direct Power Injection, DPI*) is used for EMS, while IEC61967−2 (*Measurement of radiated emissions − TEM cell and wideband TEM cell method*) and IEC61967−4 (*Measurement of conducted emissions − 1 Ω / 150 Ω direct coupling method*) are used for EMI.

Sources of Noise

Many circuits designed today must withstand certain levels of radio frequency (RF) noise. RF generators, electrostatic discharge, high−frequency switching, and power mains all play a part in electromagnetic interference. This EMI can easily be transferred to any device through EM waves, inductive/capacitive coupling, conduction, or any combination of these. One of the main roles of EMC testing in SMPS is to allow designers to optimize their design by severely limiting these interferences.

Architecture of SMPS

SMPS circuits are commonly used to translate voltage levels in many automotive applications where high−efficiency is a paramount consideration.

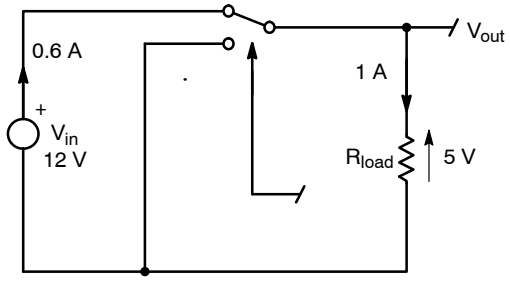

Figure 1. Switch−mode Power Supply

Unlike linear power supplies, SMPS circuits have the ability to step up (boost), step down (buck), or invert their input voltage. Figure 1 shows a basic diagram of an SMPS operation. Notice that the circuit does not constantly provide power from V_{in} to the load, which markedly increases its efficiency. A well−designed SMPS circuit can achieve an efficiency of more than 80%.

Buck converters allow for large fluctuations in input voltage while maintaining a constant output voltage.

Figure 2 depicts a single−pole double−throw switch attached to a load resistor.

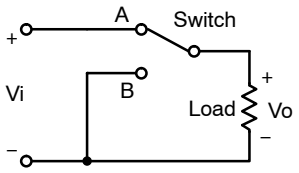

Figure 2. Switched Resistor

In position A, current is allowed to pass through the resistor. In position B, the current is cut off from the resistor, demonstrated in Figure 3.

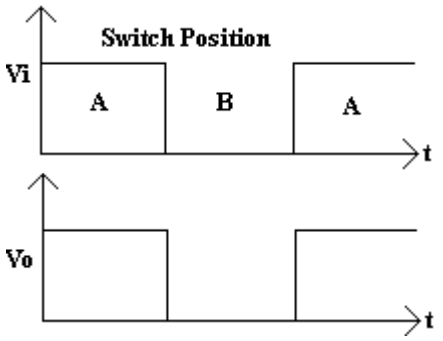

Figure 3. Output Voltage vs. Input Voltage

Given that a constant output voltage is required, an inductor can be added to smooth out the output voltage, shown in Figure 4.

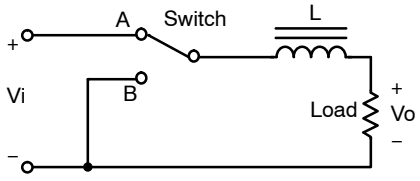

Figure 4. Inductance

Since the inductor is in series with the load resistance, the current through the two components is equal. Therefore, the inductor limits the fluctuations in current through the load, making the output voltage much more consistent. In Figure 5, the output voltage is shown to be rising and falling around an average voltage. When the switch is in position A, the current starts flowing through the circuit and charges the inductor. The inductor stores energy according to:

$$E = \frac{1}{2}LI^2$$

When the switch is in position B, the voltage supply is disconnected and the current in the inductor decreases, discharging through the circuit.

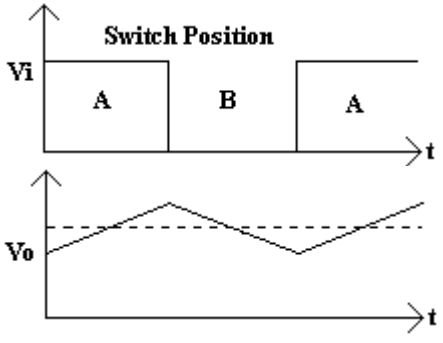

Figure 5. Average Output Voltage

A capacitor can also be added in parallel with the load to diminish fluctuations in the output voltage, as shown in Figure 6.

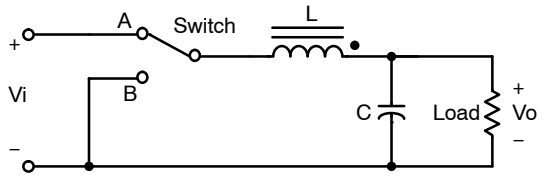

Figure 6. Capacitance

Although power can be lost through the internal resistance of the capacitor, selecting capacitors with a low effective series resistance (ESR) can minimize this concern. Energy is stored in the capacitor according to:

$$E = \frac{1}{2}CV^2$$

This LC filter that is created limits fluctuations in the current through the load as well as the voltage across the load. The result is a well controlled output voltage generated from a wide range of input voltages.

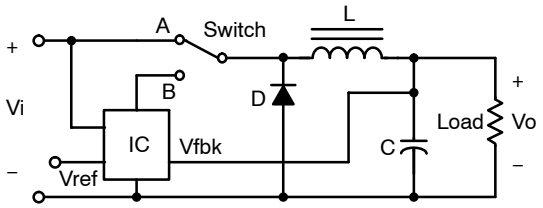

Figure 7. Buck Converter

Figure 7 shows a buck converter applied to step down a variable input voltage to a regulated output voltage. A diode is added to provide a current path during the ‘discharge’ period. To optimize efficiency, a Schottky diode is preferred. An integrated circuit (IC) is utilized to regulate the output voltage while a transistor is inserted as the switch itself.

The main drawback of SMPS is that the rapid switching creates noise, which can lead to electromagnetic interference with other devices. The next sections discuss the testing procedures for measuring the levels of interference and ways to minimize it.

Direct Power Injection

According to the International Electrotechnical Commission (IEC), all SMPS deices are required to be tested with the direct power injection method (IEC62132−4). An RF noise signal is injected into each pin of the device under test (DUT) to determine the level of disturbance at which it fails.

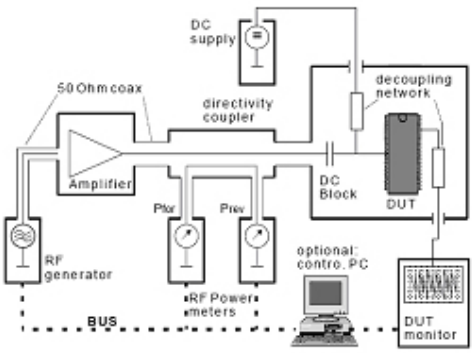

Figure 8. DPI Equipment Setup

While injecting noise into the system, an RF generator (Figure 8) is monitored by a directional coupler, measuring forward and reflected power. To reduce the reflected power through the system, uniform 50 Ω impedance is maintained throughout the cables and the printed circuit board (PCB). A 3 dB attenuator may be added before the input capacitor since the DUT may not exhibit constant impedance over the frequency spectrum of interest.

A common procedure (see Figure 9) is used to test each pin of the DUT. At each particular frequency, a power limit is set. If the device pin passes the limit, the power level is recorded and the frequency is increased. If the device pin fails, the power is decreased in 1 dB increments until it attains a passing status. At this point, the frequency is increased and the process continues. Once the incremented frequency reaches the upper limit set by the user, the test sequence for that pin in complete.

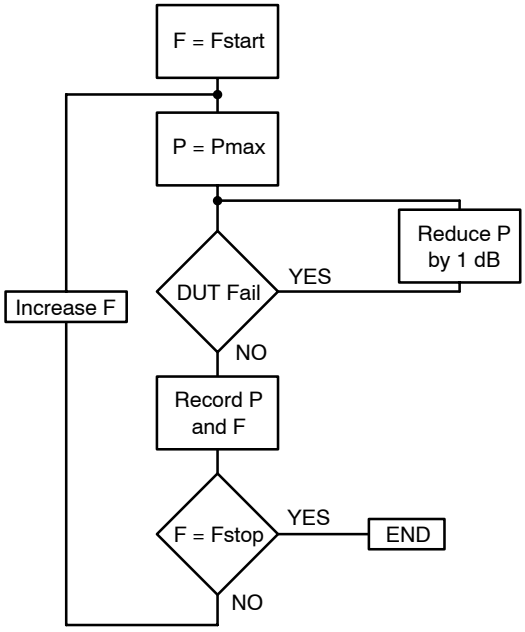

Figure 9. DPI Algorithm

The RF generator outputs a sinusoidal waveform ranging from 150 kHz to 1 GHz. The waveform is either a continuous wave (CW) or an amplitude modulated (AM) wave, with a 1 kHz, 80% modulation.

EMC Testing for SMPS: DPI

For SMPS applications, the typical DPI power level requirement for global pins is 1 W (30 dBm) and 17 dBm for local pins. A global pin carries a signal or power that enters or leaves the application board while a local pin carries a signal or power that does not leave the application board. Local pin transmissions remain on the application board as signals between two components.

With SMPS, the input and output pins are considered global pins and tested at 30 dBm. Local pin examples include: a switch pin, a boost pin, an enable pin, which are tested to the 17 dBm limit. A test configuration example is shown in Figure 10.

Method:	DPI according to IEC 62132-4
Frequency range:	1MHz to 1GHz
Frequency increment:	10% until 400MHz and 5% until 1GHz
Increment duration:	1 s
Frequency modulation:	None (continuous wave)
RF Calibration method:	Substitution
Power compliance limit:	33dBm for global pin 17dBm for local pin
Power step size:	1dBm
Device pins injected:	VIN, VOUT, VSW
Device pins monitored:	VOUT, VSW
Load resistance:	250 Ω
DC input voltage:	12 V
Acceptance criteria:	Output voltage within 4% of nominal value Digital outputs remain in correct state ±1V

Figure 10. Test Conditions

A DPI test setup for an SMPS printed circuit board is shown below:

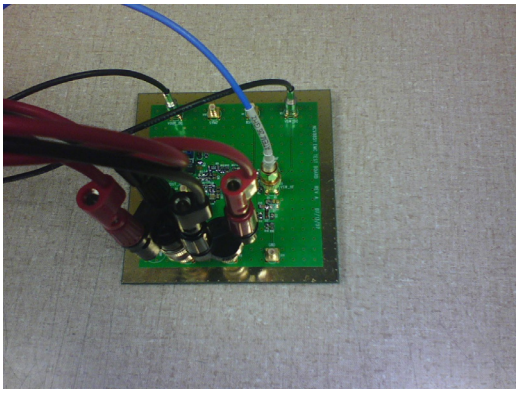

Figure 11. Sample DPI Test Configuration

Figure 12 shows an example of the failure criteria set up on an oscilloscope. If the monitored signal deviates from the overlaid mask, a ‘failure’ status is sent to the computer and the power level is decreased.

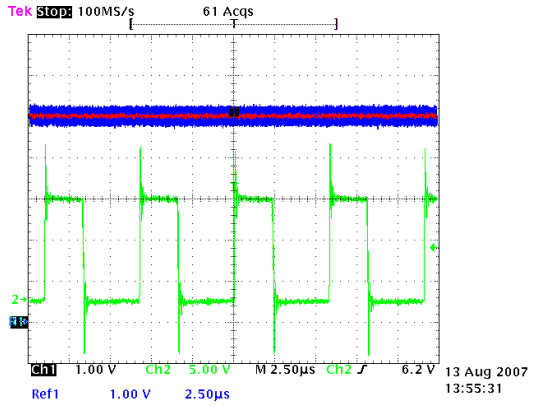

Figure 12. Failure Criteria

In Figure 13, a failure on the input pin has occurred because the output voltage has risen above the failure mask.

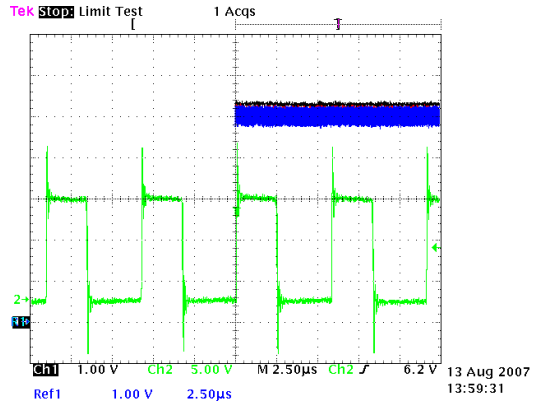

Figure 13. Failure on the VIN Pin

Differential Conducted Emission

All SMPS devices are required to be tested under the 1 Ω / 150 Ω direct coupling method (IEC61967−4). Commonly referred to as differential conducted emission (DCE), the device noise is monitored on each pin to determine the level of electromagnetic emission.

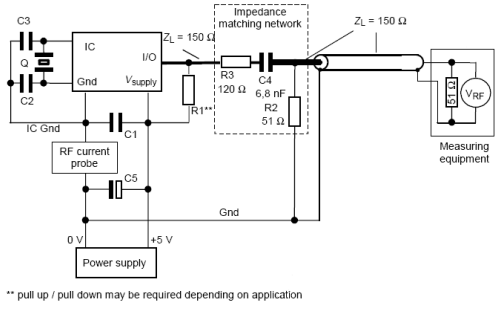

Figure 14. DCE Equipment Setup

Unlike DPI, where power was *injected* into each pin, DCE simply monitors the level of radiation emitted from each pin. To accurately measure this emission, an impedance−matching network is necessary between the pin being monitored and the measuring equipment.

Once the impedance−matching networks and equipment are connected, each pin of the DUT can be tested for DCE. Note that the ground pin is treated differently from other pins. Instead of a 150 Ω impedance−matching network, a 1 Ω probe (Figure 15) is attached between the device ground and the system ground to detect the voltage drop across the 1 Ω current sense resistor.

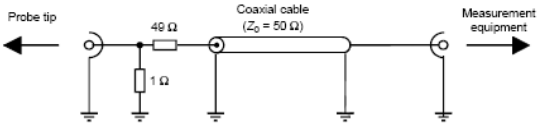

Figure 15. 1 Ω Probe Setup

EMC Testing for SMPS: DCE

Typical requirements for the 150 Ω method for automotive applications are shown below in Figure 16.

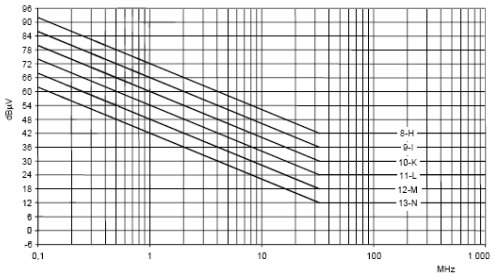

Figure 16. 150 Ω − Reference Levels for Automotive Applications

The unit ‘dBµV’ represents a level 107 dB less than the ‘dBm’ level. Although just six levels are shown, some applications may require different reference levels, which are included in the IEC61967−4 standard. These levels represent the maximum emission that is acceptable from each pin of the DUT.

When the ground pin is being tested with the 1 Ω probe, it is held to a much more rigorous standard, as shown in Figure 17. The lowest reference level in this standard drops to 0 dBµV after 30 MHz.

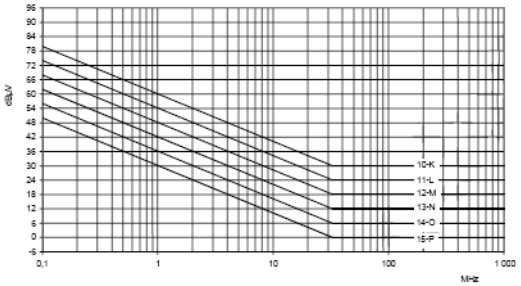

Figure 17. 1 Ω − Reference Levels for Automotive Applications

For DCE testing in SMPS, there are no local or global pin considerations. All pins are tested equally and held to the same standards. A typical example of a test configuration is shown in Figure 18.

Method:	DCE according to IEC 61967-4
DC input voltage:	12 V
Spectrum Analyzer Parameters:	
Frequency bandwidth:	100kHz to 1GHz
RBW:	10kHz
VBW:	30kHz
Reference Level:	107dBμV
Attenuation:	10dB
Device pins monitored:	VIN, VOUT, VSW, BST
Load resistance:	250 Ω
Acceptance criteria:	Emission below reference levels in *Figure 15*

Figure 18. Test Conditions

Emissions are typically measured from 100 kHz to 1 GHz with a load attached to simulate real circuit conditions. A common DPI setup for an SMPS printed circuit board is pictured below:

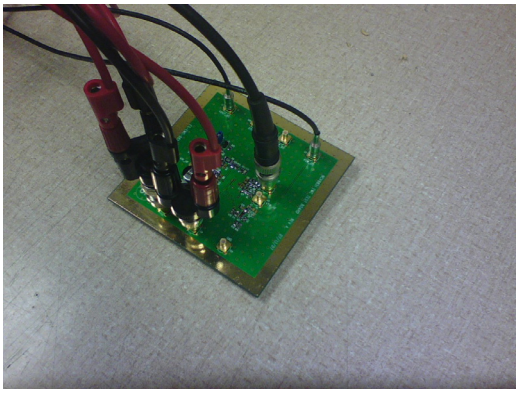

Figure 19. Sample DCE Test Configuration

The noise from each pin is often compared to the background noise of the equipment, as shown in Figure 20. This is to isolate the actual emission from each pin.

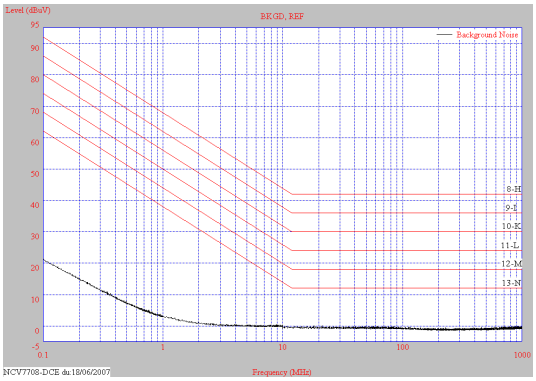

Figure 20. Background Noise

When an SMPS device is in operation, its switching signal is a square waveform. Since the square wave is in the time−domain, it must be converted to frequency−domain so that the spectrum analyzer can measure it.

When a pure sine wave, 1 GHz, for example, is transformed into frequency−domain using Fourier analysis, a single spike is shown on the graph at 1 GHz, in our case. When a square wave is transformed into the frequency−domain, a large spike is shown at the fundamental frequency (the frequency of the original waveform) and other spikes are produced at the odd harmonics (odd multiples) of the waveform.

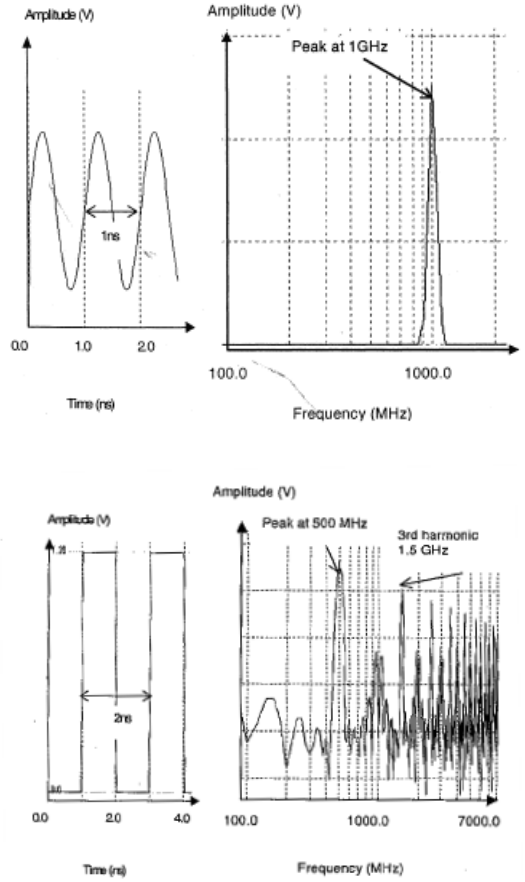

Figure 21. Time / Frequency−Domain Comparison

If a 1 GHz square wave were transformed into frequency−domain, a spike would appear at 1 GHz, 3 GHz (3rd harmonic), 5 GHz (5th harmonic), etc. These harmonics will be observed in later sections with the fundamental frequency of the SMPS device.

Transverse Electromagnetic Mode

Per IEC requirements, all SMPS devices are tested under the TEM cell method (IEC61967−2). This method measures the radiated emissions from the DUT at short distances. To perform this test, the DUT is mounted on the bottom of a 10 cm x 10 cm four−layer PCB with all traces and other components on the other three layers, as shown in Figure 22.

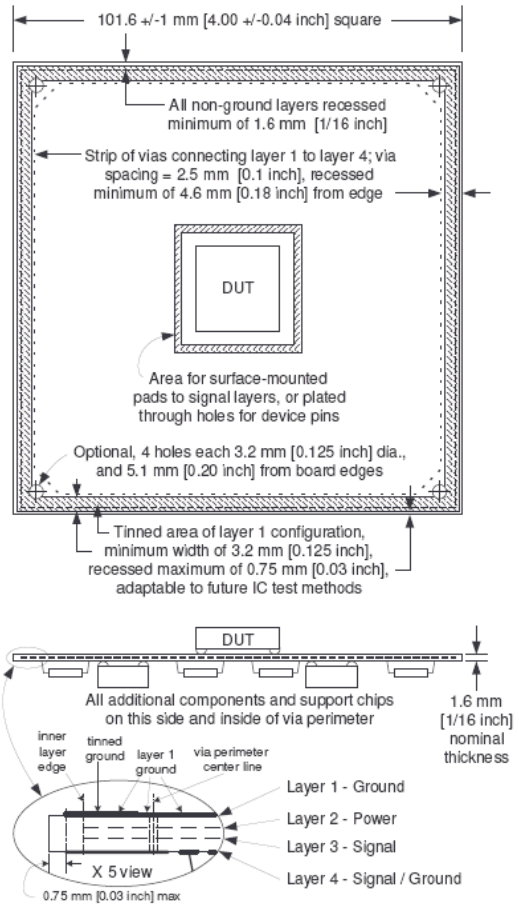

Figure 22. PCB Setup

This assures that the measured electromagnetic radiation is due solely to the IC. The PCB is then mounted to the TEM cell device with the IC on the inside and connections made as shown in Figure 23. The system ground layer is exposed on the edge of the PCB so that it makes a connection with the opening in the TEM cell. This creates a ‘sealed,’ or continuous, environment within which the device can be tested.

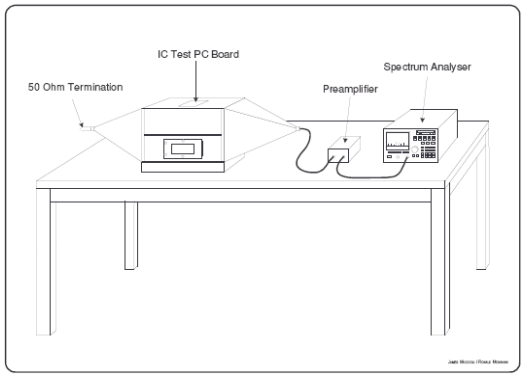

Figure 23. TEM Cell Setup

The TEM cell is connected to a spectrum analyzer via a 50 Ω cable (again to make the impedance uniform) and the device is measured for radiated emission. The test is then repeated with the PCB rotated 90° from its original orientation. All four orientations must be tested so that the orientation with the greatest emission can be the one taken into consideration for design improvements.

EMC Testing for SMPS: TEM Cell

Typical reference levels for TEM emission are shown in Figure 24.

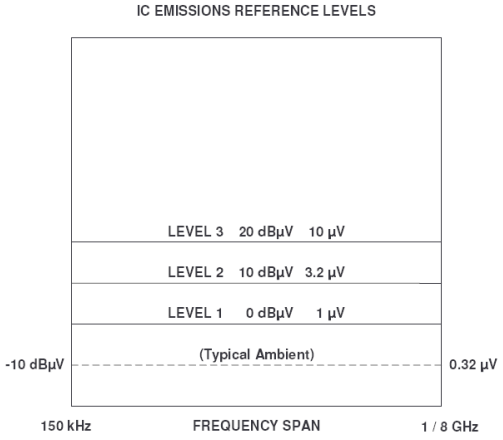

Figure 24. Reference Levels

Again, the unit ‘dBµV’ represents 107 dB less than the ‘dBm’ unit.

For TEM cell testing, there are no individual pin considerations because we are only concerned directly with the overall IC radiated emission. Figure 25 shows a typical configuration for a TEM cell test.

Method:	TEM cell according to IEC 61967-2
DC input voltage:	12 V
Spectrum Analyzer Parameters:	
Frequency bandwidth:	150kHz to 1GHz
RBW:	10kHz
VBW:	30kHz
Reference Level:	107dBµV
Attenuation:	10dB
Load resistance:	250 Ω
Acceptance criteria:	Emission below reference levels in *Figure 23*

Figure 25. Test Conditions

A common TEM cell setup for an SMPS printed circuit board is shown below:

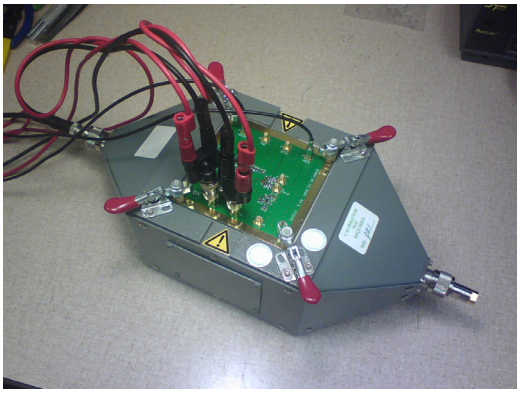

Figure 26. Sample TEM Test Configuration

The ambient system noise must be at least 6 dB below the intended reference level to receive an accurate measurement. This background noise can be measured by replacing the PCB with a metal plate to completely enclose the TEM cell, shown in Figure 27.

Figure 27. Sealed TEM Cell

Typical Demo Board with Results

A synchronous buck controller was placed on a demo board to demonstrate the EMC qualities of the device. Although a 12 V input will be used to test the device, it is capable of input voltages ranging from 4.5 V to 40 V.

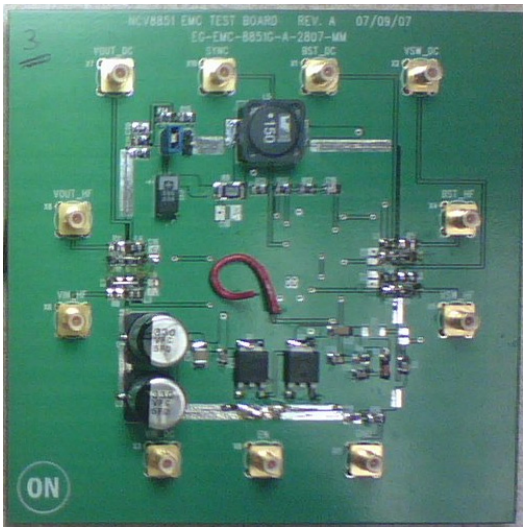

Figure 28. Layout A

Figure 28 shows a 2−layer board that wasn't designed with any specific rules in mind. It was simply laid out in an organized fashion. The square area in the middle of the board is the device ground. The device ground is separated from the outer system ground so that DCE testing can be done on the ground pin. The exposed area of both ground sections allows them to be connected for further DCE tests and DPI testing.

The following curve resulted when the DCE test was performed on the ground pin:

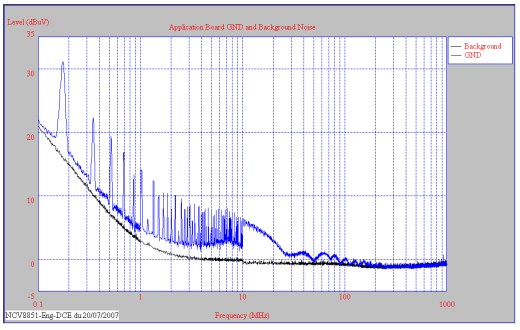

Figure 29. DCE on Ground Pin

Notice the spike at about 170 kHz along with its associated harmonics. The noise is generated mainly from the switching of the device, which is set at 170 kHz in this particular setup. Also take note that the black trace represents the background noise level, which is noise generated from the equipment and inside the room. This level is measured with the device powered up, but disabled.

The following graph depicts the ground pin emission with the reference levels superimposed on the graph:

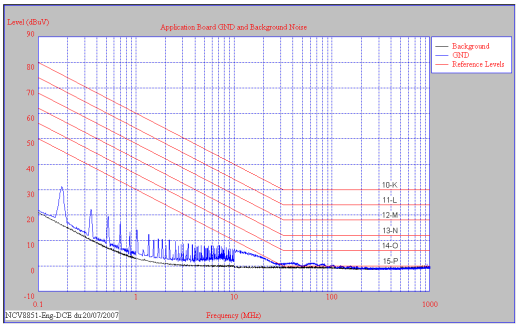

Figure 30. DCE on Ground Pin

The emission from the ground pin (see Figure 30) fails to meet the 15−P reference level requirement between 30 MHz and 100 MHz.

The following curve resulted from a DCE test on the output (V_{OUT}) pin:

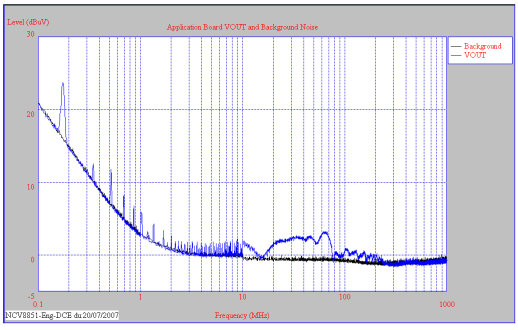

Figure 31. DCE on V_{OUT} Pin

Once again, a spike is shown at the switching frequency (170 kHz) as well as the relative harmonics. The emission on the V_{OUT} pin passes all reference levels for automotive applications, as shown below:

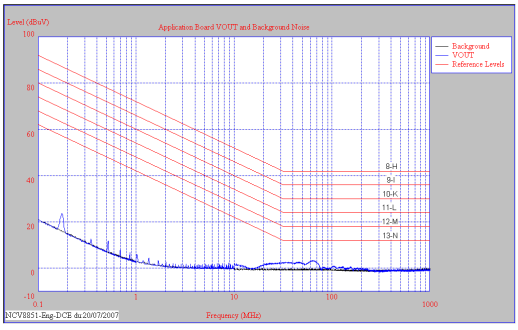

Figure 32. DCE on V_{OUT} Pin

Although this pin passes all of the reference levels, it can still improved by following some guidelines in the design process of the PCB, discussed in the next section.

The following curve resulted from a DPI test on the V_{IN} pin of the DUT at 33 dBm:

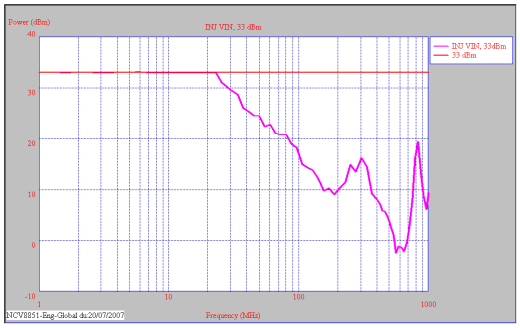

Figure 33. DPI on V_{IN} Pin

The device begins to fail at about 25 MHz until 1 GHz. Notice that the susceptibility of the device peaks at 650 MHz reaching only −2 dBm.

The result of the V_{OUT} pin injection of the DUT is shown below:

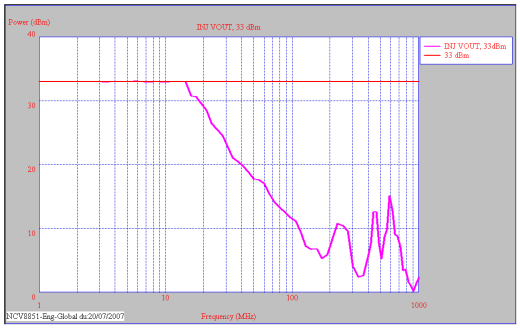

Figure 34. DPI on V_{OUT} Pin

Similarly, the device begins to fail the 33 dBm power limit at about 15 MHz until 1 GHz. The susceptibility of the V_{OUT} pin peaks at 900 MHz and 0 dBm.

PCB Guidelines

A variety of rules and guidelines must be considered when designing a PCB for EMC testing. The board itself should a four−layer board with signal traces on the top and bottom layers. The middle two layers should be a device ground plane and a power plane, as shown below:

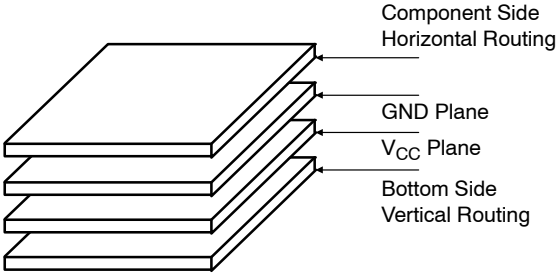

Figure 35. PCB Board Layers

All components on the PCB should be placed into functional groups. For example: an analog group, a digital group, and a power supply group (see Figure 36) could be used. This is critical in reducing interference and crosstalk.

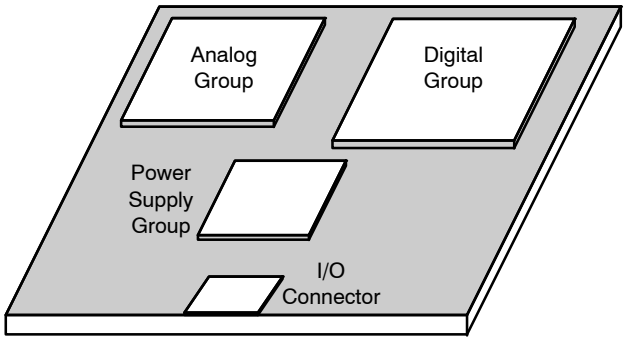

Figure 36. PCB Functional Groups

All ground connections must be made directly to the ground plane to prevent ground loops. Loops can produce large amounts of radiated emission, which is unfavorable for EMC. Slots and bottlenecks should be avoided as well, as shown below:

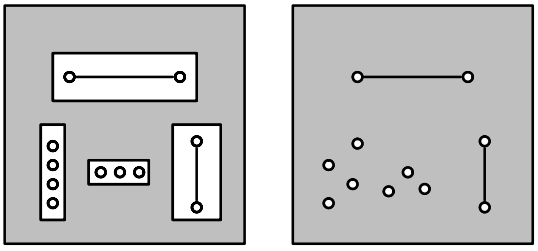

Figure 37. PCB Ground Patterns

All vias should be separated so that there is at least 1 mm of ground space between them. Slots can be avoided by simply arranging the vias in a zigzag pattern. Note that the length / width ratio of the PCB must be less than 5 to minimize the inductance of the ground plane.

Parasitic elements can reduce the functionality of an IC on a poorly designed PCB. The parasitic inductance of a trace in comparison to length is shown below:

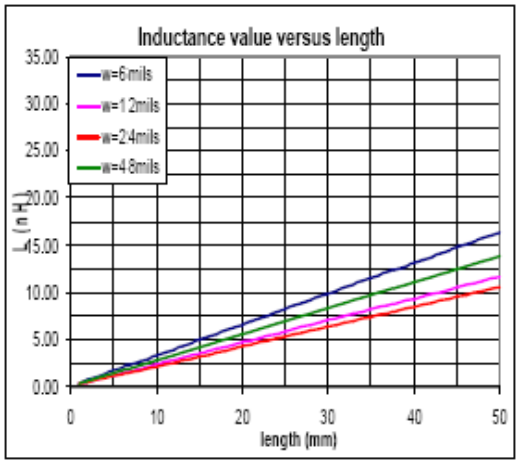

Figure 38. Parasitic Inductance vs. Trace Length with 90 μm Layer Spacing

Figure 38 shows that a shorter trace reduces the amount of parasitic inductance through it. Using the following equation, parasitic inductance can be calculated, where l is the length of the trace, w is the width of the trace, h, is the distance between the trace and the neighboring plane, and L_f is the parasitic inductance. All dimensions are in mm and the inductance is in nH.

$$L_f = 0.2 \cdot l \cdot \ln\left[\left(\frac{8 \cdot h}{w}\right) + \left(\frac{w}{4h}\right)\right]$$

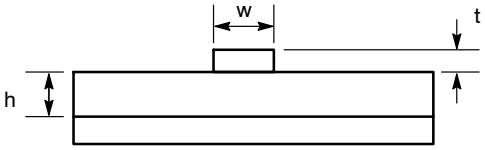

Figure 39. Parasitic Inductance

Parasitic capacitance also increases with trace length, as shown in Figure 40.

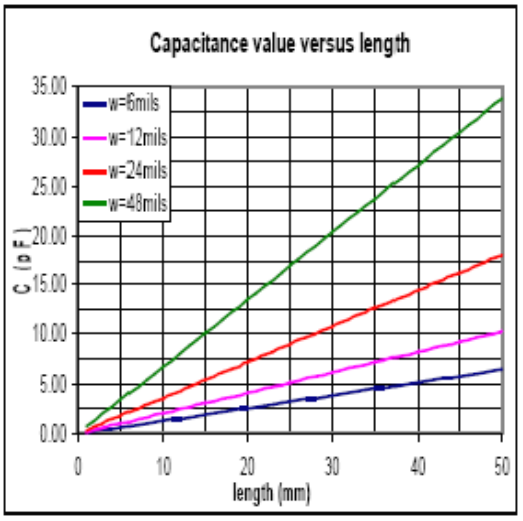

Figure 40. Parasitic Capacitance vs. Trace Length

Notice that a wider trace produces more parasitic capacitance. The parasitic inductance of a trace in comparison to width is shown in Figure 41.

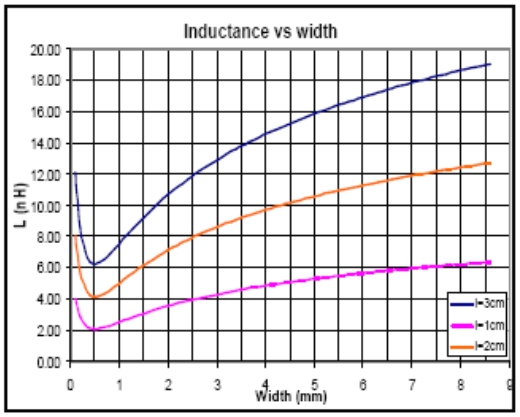

Figure 41. Parasitic Inductance vs. Trace Width

A wider trace width does not always provide for a lower parasitic inductance. The optimal trace width is 0.495 mm, or 20 mils.

Trace orientation is another important consideration in EMC testing. Angles less than forty−five degrees must be used to prevent signal reflection. When ninety degree angles or greater are used, high frequency signals are reflected back through the trace. Reflection causes a change in the waveform and produces inaccurate results. Traces with high switching current should also be placed at least 3 mm away from other parallel signal traces.

Device decoupling capacitors must be placed very close (less than 1 mm preferred) to the V_{CC} and GND pins of the IC to reduce the amount of parasitic inductance through the trace. The EMC networks for DCE testing must be placed very close to their corresponding pins for the same reason.

Bulk capacitors must be decoupled with a smaller capacitor with a lower effective series inductance (ESL). The smaller value capacitor should be placed closest to the particular device pin. High−frequency, low−inductance ceramic decoupling capacitors should be used on each power pin. 0.1 μF capacitors should be used for lower frequencies (below 15 MHz) and 0.01 μF capacitors should be used for higher frequency applications (above 15 MHz).

Favorable results can be produced once all of these guidelines are used in the PCB design process.

EMC Board with Results

The same synchronous buck controller that was tested in the previous section was also tested on a board that followed strict EMC guidelines, as shown below:

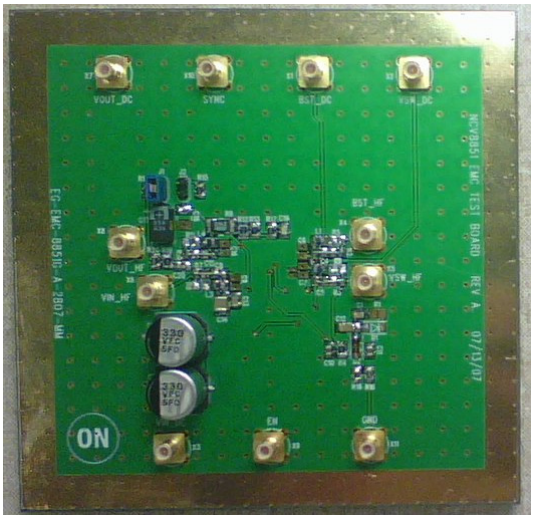

Figure 42. Layout B

Notice that the external components and connectors are placed very close to the device, which is mounted on the underside of the board. All traces were made as short as possible with a width of 20 mils. The connectors on the outer edge of the board allow for longer traces because they contain only DC signals.

The results from the DCE test performed on the GND pin of the new device setup are shown below:

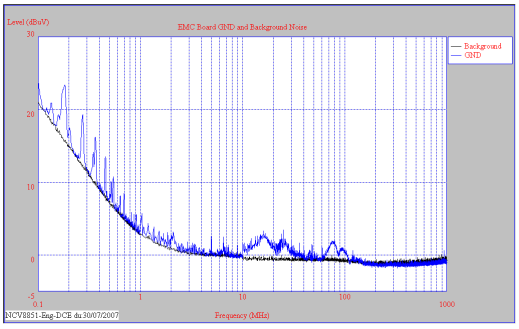

Figure 43. DCE on GND Pin

Again, notice the spike at 170 kHz due to the switching frequency. The same graph with added reference levels is shown in Figure 44.

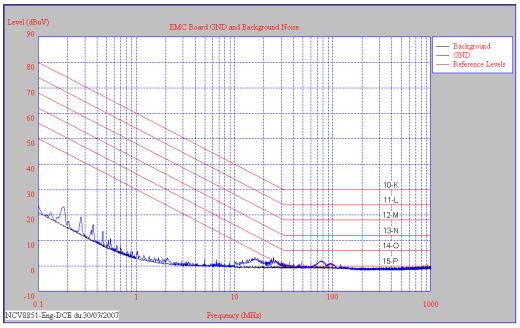

Figure 44. DCE on GND Pin

Figure 45 shows the comparison between the emissions of the two boards.

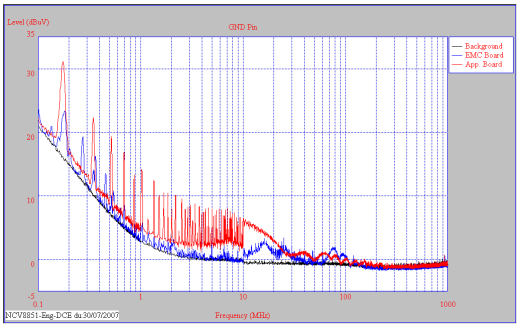

Figure 45. DCE on GND Pin Comparison

Although the emission from the ground pin on the optimized board layout does not pass, it is greatly improved over that from the demo board layout. The emission from the V_{OUT} pin on the improved board produced the following curve:

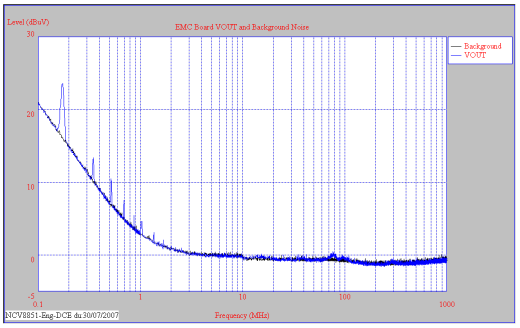

Figure 46. DCE on V_{OUT} Pin

The spike at 170 kHz is still shown, but the overall emission from the pin is significantly reduced. Figure 47 shows emission from V_{OUT} compared to the reference levels:

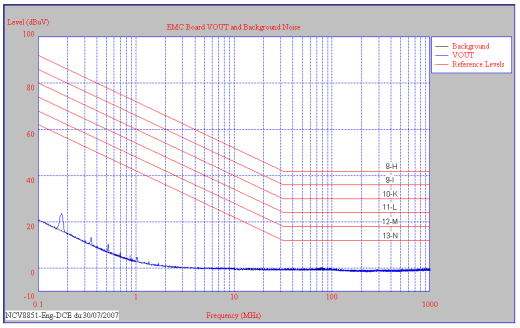

Figure 47. DCE on V_{OUT} Pin

The emission of both boards from the V_{OUT} pin is shown in Figure 48, below.

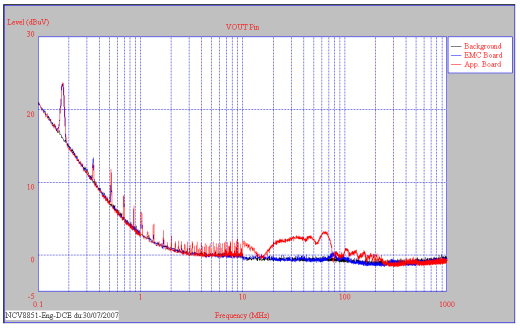

Figure 48. DCE on V_{OUT} Pin Comparison

Take special note of the improvements between 10 MHz and 300 MHz. The new board layout greatly decreased the emission from the V_{OUT} pin.

The following curve resulted from a DPI test on the V_{IN} pin of the DUT at 33 dBm:

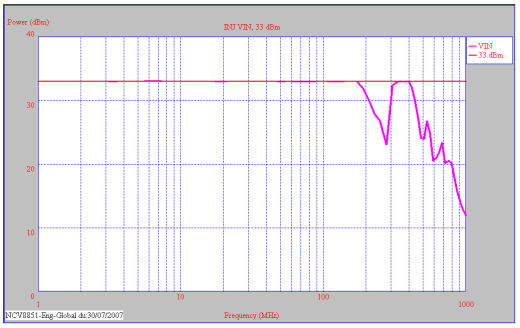

Figure 49. DPI on V_{IN} Pin

Susceptibilities were measured from 180 MHz to 330 MHz and from 400 MHz to 1 GHz. The susceptibility of the V_{IN} pin peaks at 1 GHz with a 12 dBm power limit.

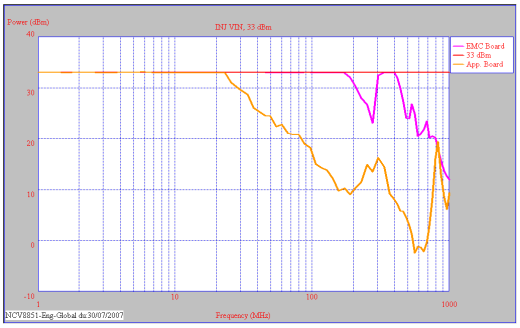

Figure 50. DPI on V_{IN} Pin Comparison

The results are not passing, but they are a significant improvement (up to 23 dBm) over the results from the demo board between 15 MHz and 800 MHz, shown in Figure 50.

A DPI test at 33 dBm on the V_{OUT} pin of the device produced the following curve:

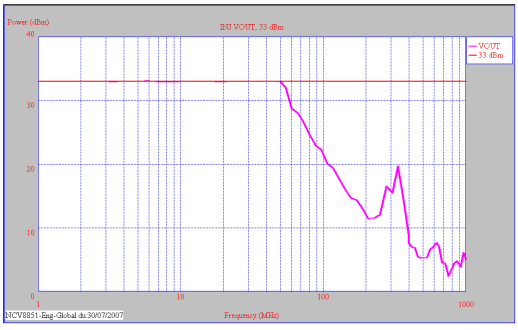

Figure 51. DPI on V_{OUT} Pin

The pin failed to meet the 33 dBm power limit starting at 50 MHz until 1 GHz. The peak of the susceptibility occurred at 750 MHz and only reached 2 dBm.

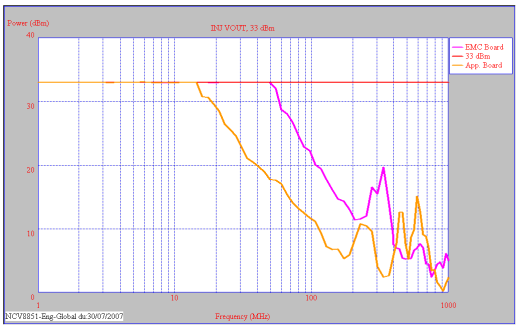

Figure 52. DPI on V_{OUT} Pin Comparison

The results from the EMC board showed a large improvement (up to 15 dBm) over the demo board between 15 MHz and 400 MHz.

Up until this point, no decoupling capacitors have been added to the input or output pins. The next section illustrates the outcome with the addition of decoupling capacitors on the input and output pins.

EBC Board and Decoupling Capacitors with Results

Injected noise can be hindered through the use of a decoupling capacitor. As the *PCB Guidelines* section discusses, it is important to place this capacitor as close to the pin as possible. Shorter traces provide more accurate results. Observe the results from the DPI test performed on the input pin with a 1 nF decoupling capacitor in place in Figure 53.

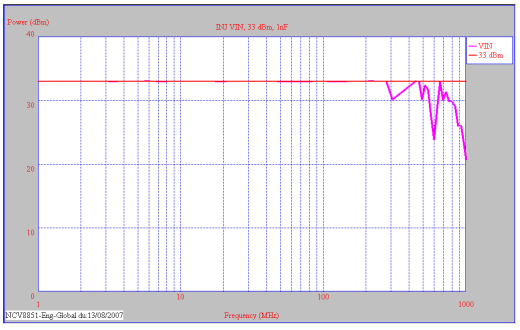

Figure 53. DPI on V_{IN} w/ 1 nF Cap

The susceptibility of the input pin to conducted RF signals is greatly reduced with the use of this decoupling capacitor, shown in Figure 54. The susceptibility is improved between 400 MHz and 1 GHz up to 10 dBm.

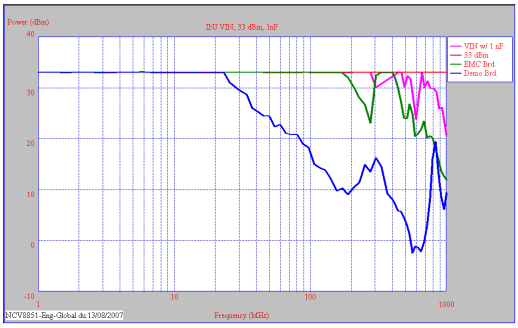

Figure 54. DPI on V_{IN} Comparison

The results from, the DPI test on the output pin with a 1 nF decoupling capacitor are shown below:

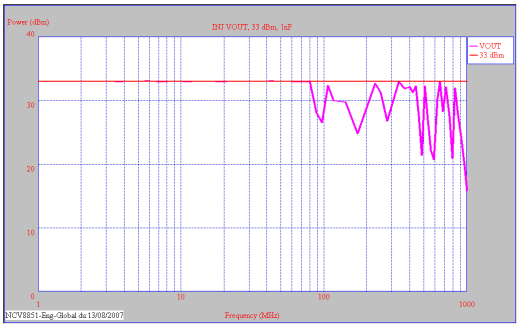

Figure 55. DPI on V_{OUT} w/ 1 nF Cap

The results are improved from 50 MHz to 1 GHz up to 20 dBm.

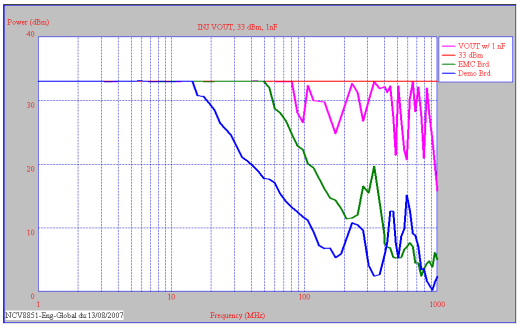

Figure 56. DPI on V_{OUT} Comparison

Conclusion

Electromagnetic compatibility is becoming an increasingly important consideration with today's faster and smaller devices. The ability of each device to function properly under its normal operating conditions without disturbing the operation of any other devices is crucial. Devices must be able to withstand disturbances (EMS) from radio frequency noise such as mains voltages or electrostatic discharges. Electromagnetic susceptibility can be tested through the direct power injection method (IEC 62132−4). They must also, at the same time, minimize their own interference (EMI) with other devices from high−frequency switching, for example. Electromagnetic interference, or emission, can be tested through the differential conducted emission method (IEC 61967−4) as well as the transverse electromagnetic cell method (IEC 61967−2).

Switch−mode power supply devices are critical power management components in many automotive applications. With their ability to step up, step down, or invert their input voltages, SMPS circuits generate a lot of unwanted noise. The noise can be hindered by following the *PCB Guidelines* discussed in this application note. Some things to consider when designing a PCB include: utilizing all layers of a four layer board, keeping traces as short as possible and restricting their widths to exactly 20 mils to reduce parasitic inductance, avoiding sharp trace angles to minimize high frequency signal reflection, and organizing the components into functional groups to decrease their crosstalk interference.

Through the use of a loosely designed demo board, a strictly designed EMC board, and an EMC board with decoupling capacitors, the design guidelines were put to the test. In the end, it was shown that the *PCB Guidelines* greatly improve the overall results of the device on a PCB. These design considerations can strongly improve the EMC test results and could mean the difference between a failed test and a passed test.

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[6] Switch Mode Power Supply. Power Designers. 11 July 2007 <http://www.powerdesigners.com/InfoWeb/resources/pe_html/ch07s1/intro.html>.

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